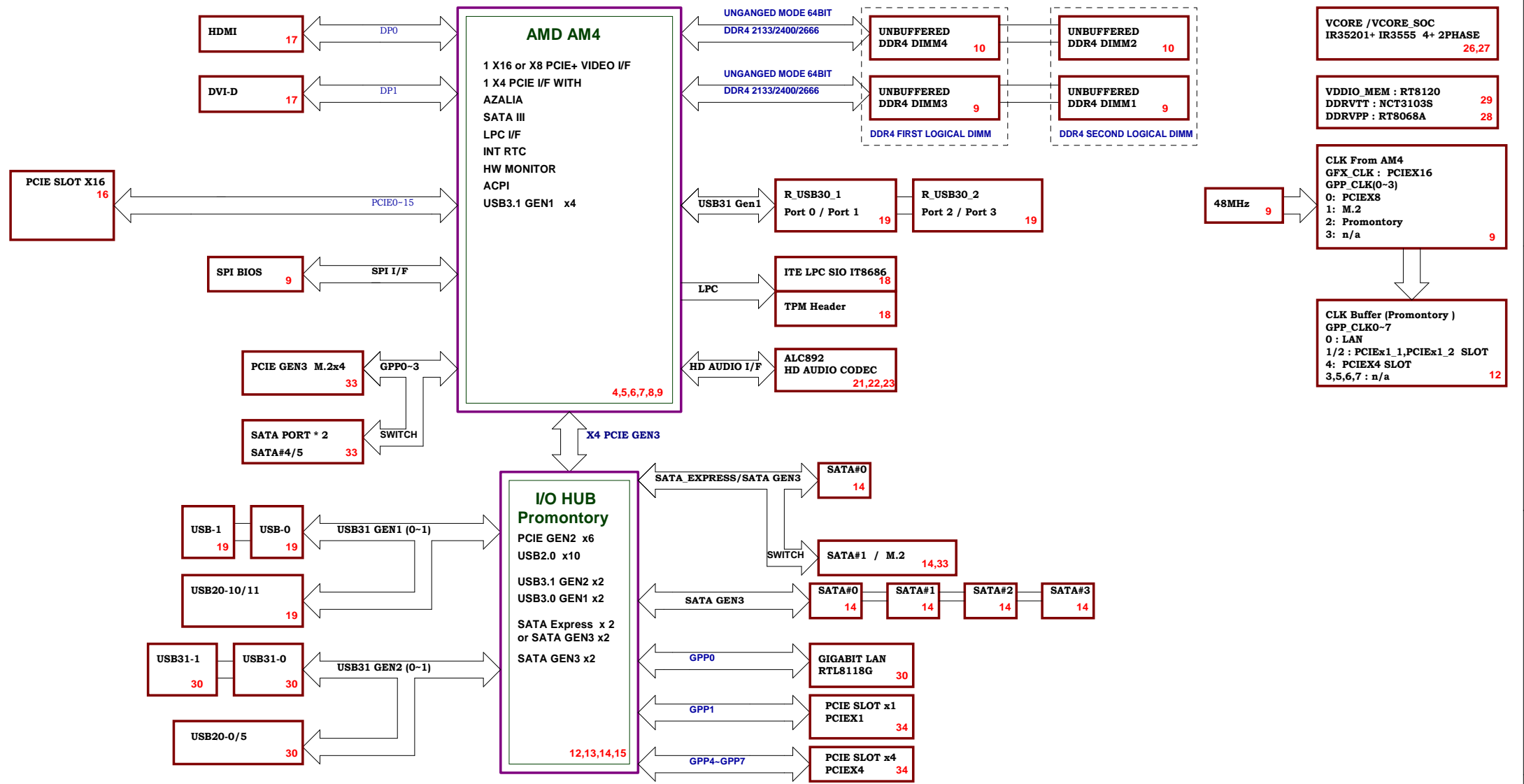


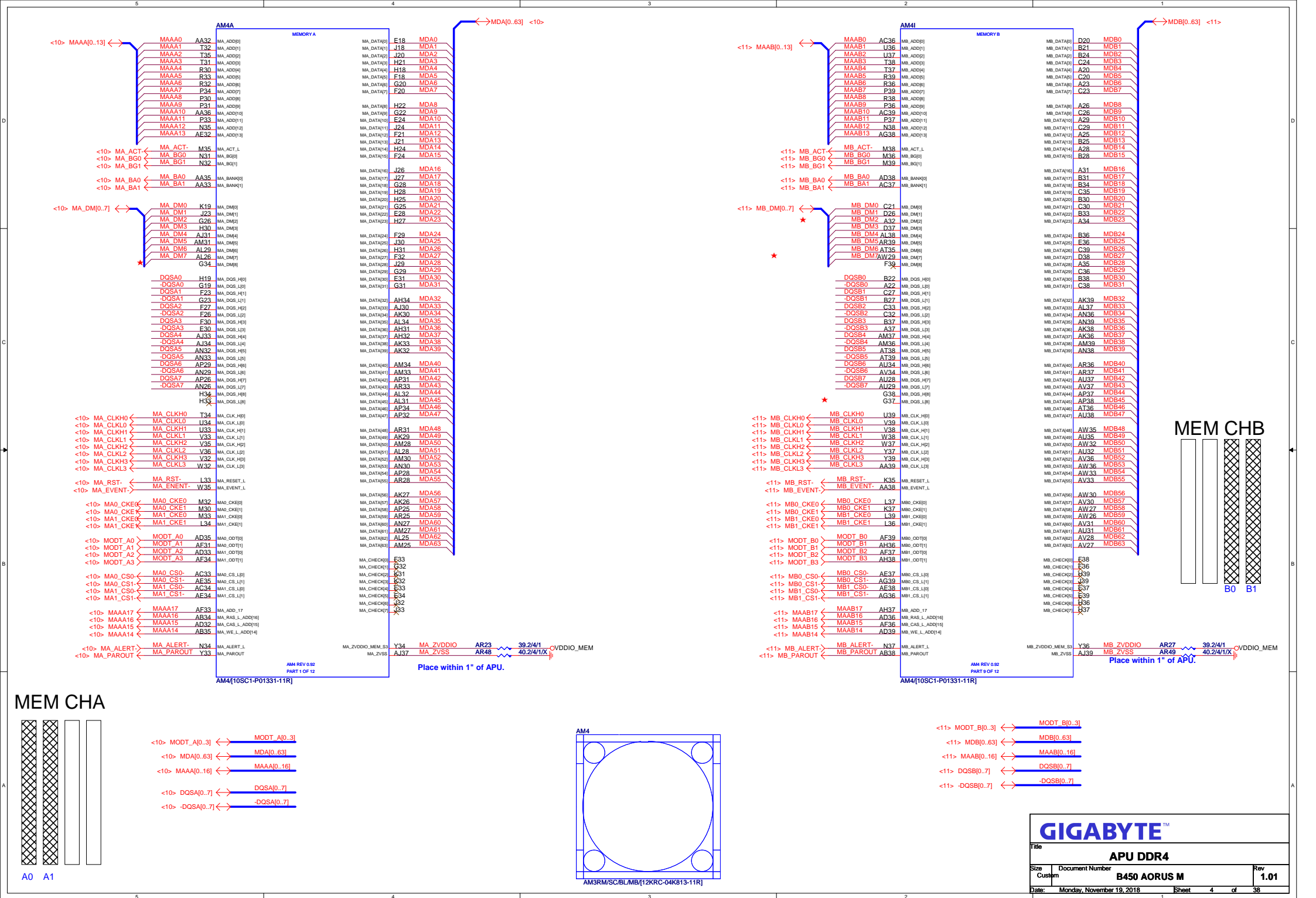
# B450 AORUS M

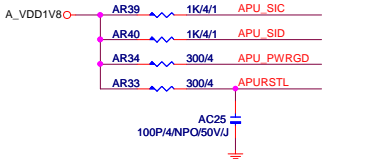
PAGE	TITLE	Revision : 1.01
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	HDMI , DVI	
18	IT8686CX , TPM	
19	F_USB30 , R_USB30 , F_USB20	
20	A_VDD1V8 / A_VDDPS5	
21	ALC892 CODEC	
22	AUDIO JACK	
23	AUDIO LED	
24	POWER SEQUENCE , A_VDDP	
25	PWM SL95712	

[illegible]

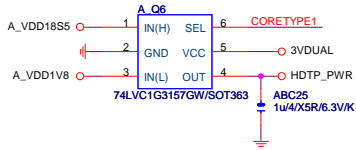
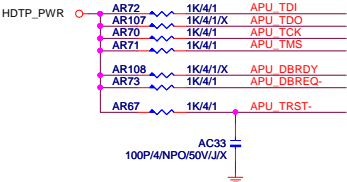
[illegible][illegible][illegible][illegible][illegible][illegible][illegible]





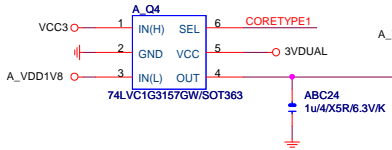
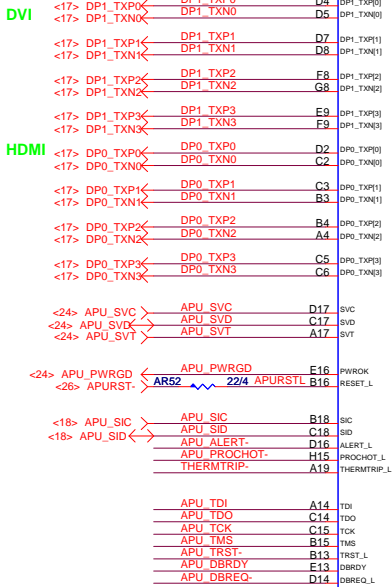


SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

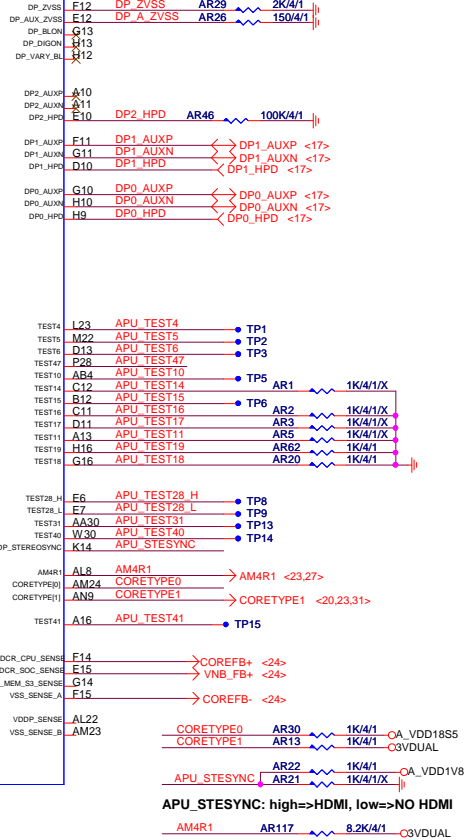


DVI

HDMI



Placed within 1500 mils from APU



AM4 CPU CoreType

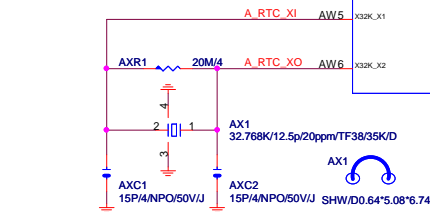
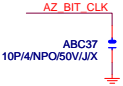
CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

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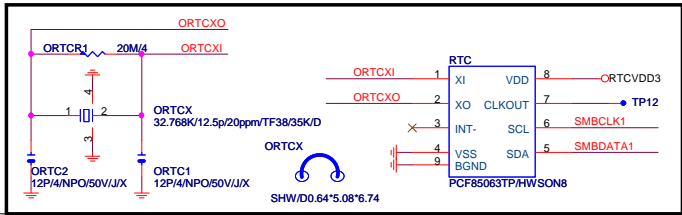
CPU CONTROL		
Title	Document Number	Rev
	B450 AORUS M	1.01
Date:	Monday, November 19, 2018	Sheet 5 of 38



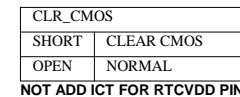
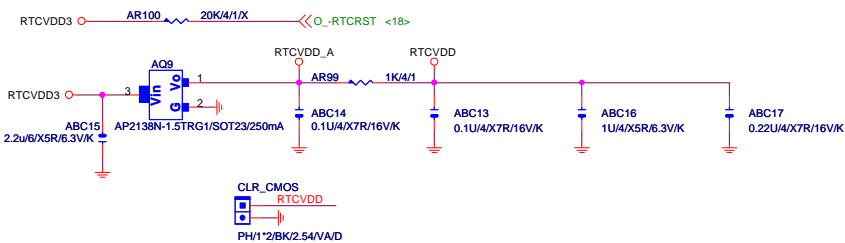
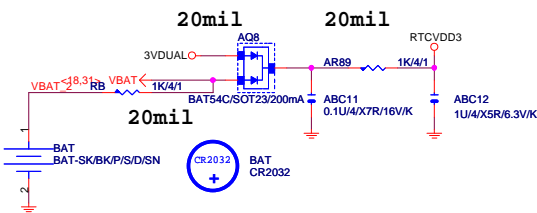
Internal Debug Only			
TEST0	TEST1	TEST2	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



	LPC_CLK0	LPC_CLK1	AGPIO3	RTC_CLK	LFRAME_L	SYS_RST#	SPI_CLK (ZP)
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48KHz crystal clock and generate both internal and external clocks (DEFAULT)	Enhanced reset logic (for quicker S5 S5 resume) (DEFAULT)	Coin battery is on board. (DEFAULT)	SPI ROM (DEFAULT)	normal reset mode (DEFAULT)	Use 48KHz crystal clock and generate both internal and external clocks (DEFAULT)
PULL LOW	BOOT FAIL TIMER DISABLED (DEFAULT)	Use 100KHz PCIE clock as reference clock and generate internal clocks only	Default to traditional reset logic (DEFAULT)	Coin battery is not on board.	LPC ROM	short reset mode	Use 100KHz PCIE clock as reference clock and generate internal clocks only
C3/ST DIE ONLY							ZP DIE ONLY

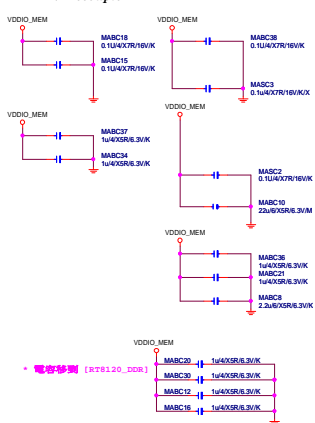


GIGABYTE™			
Title			
AM4 MISC			
Size	Document Number	Rev	
Custom	B450 AORUS M	1.01	
Date:	Monday, November 19, 2018	Sheet	7 of 38

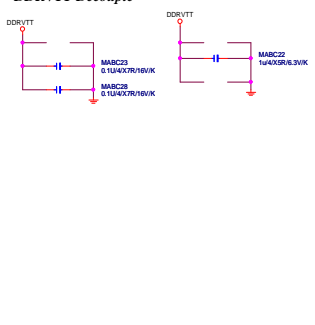




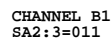
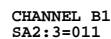


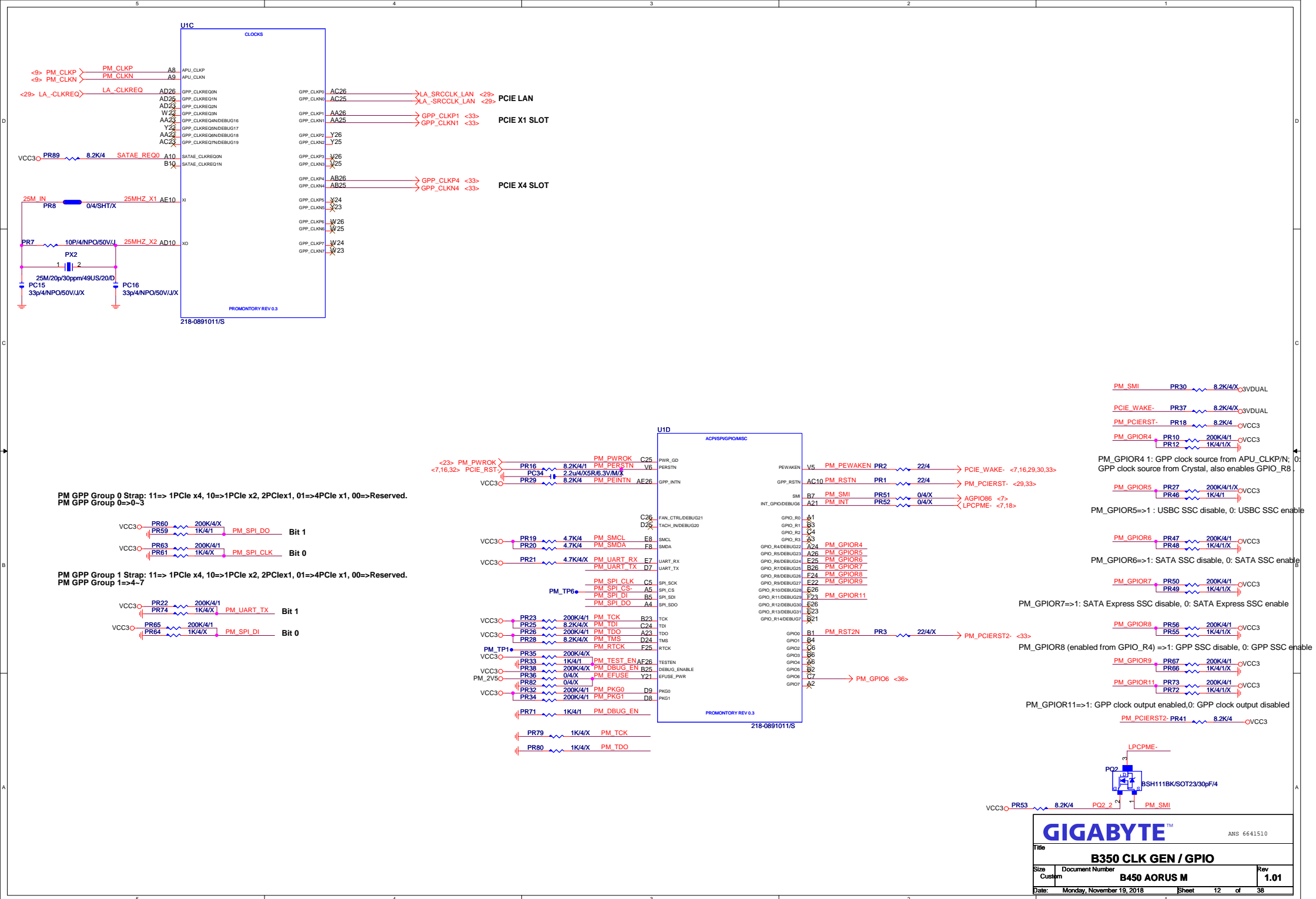


### DDRVTT Decouple



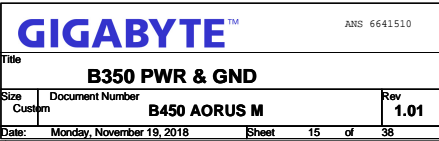
teknisi-indonesia.com



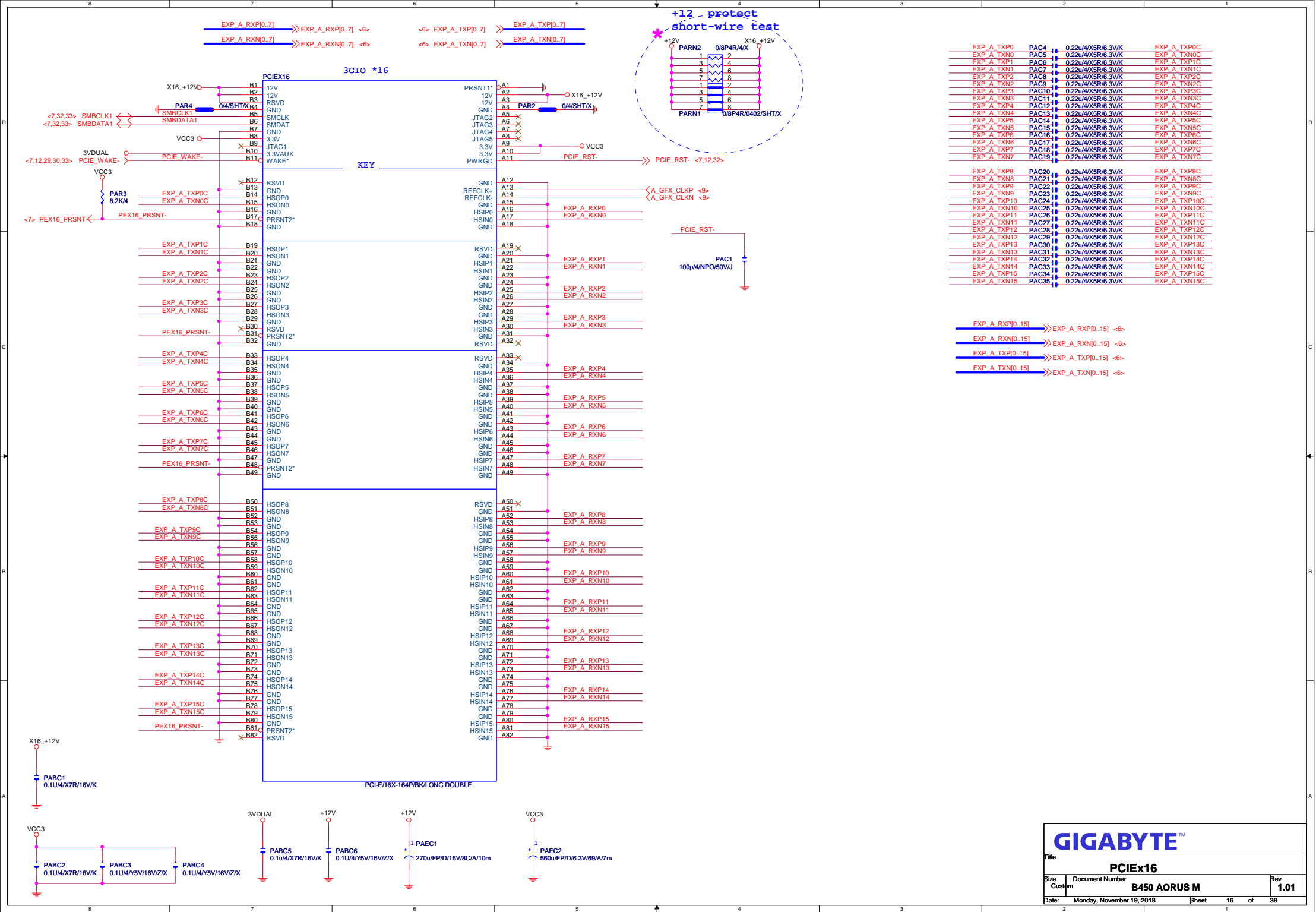




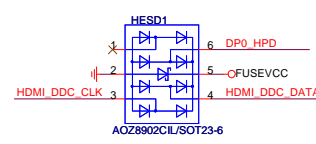
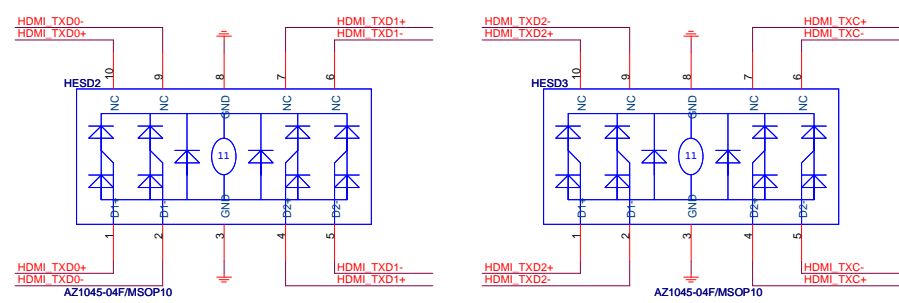
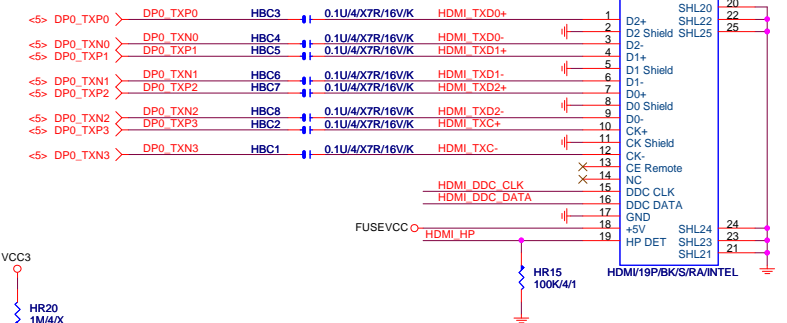
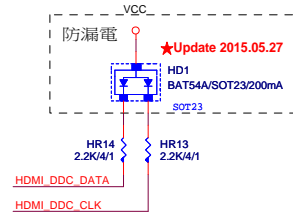
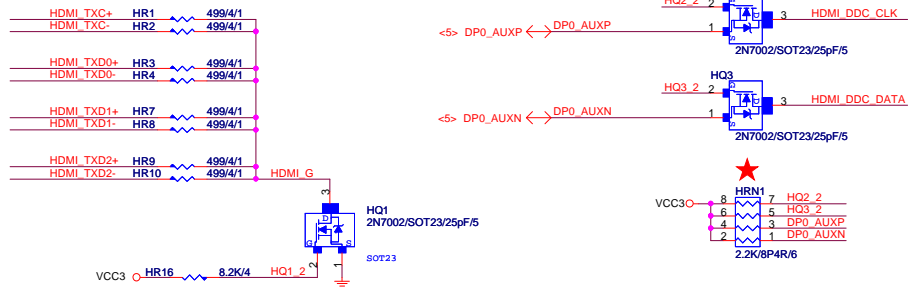








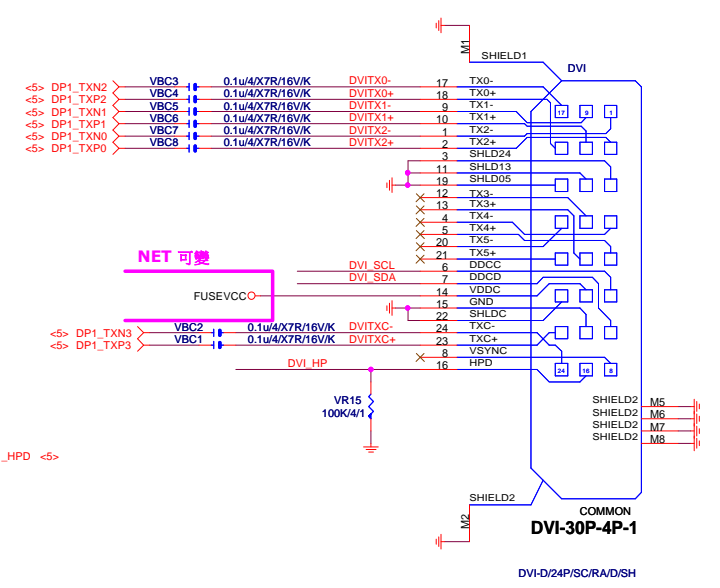
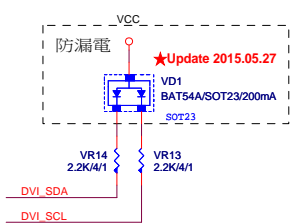
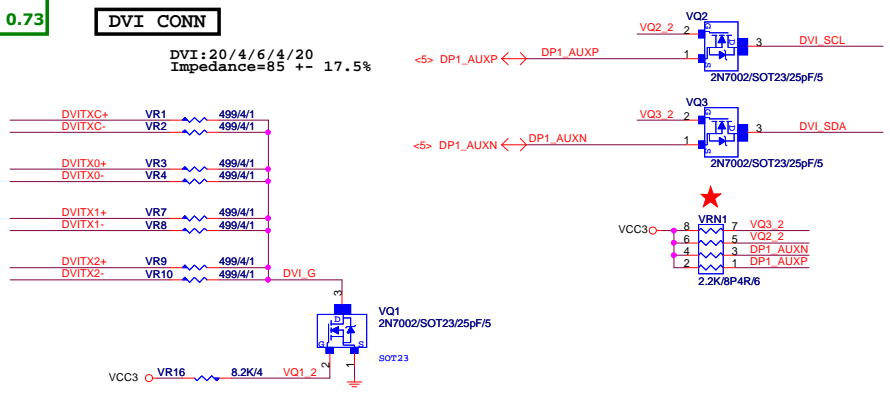




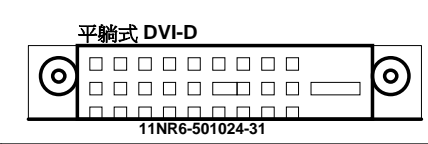
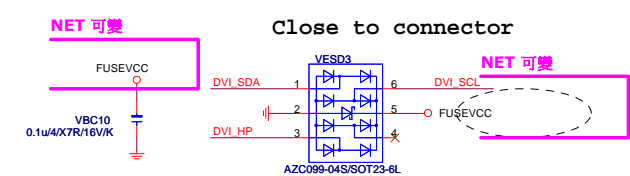
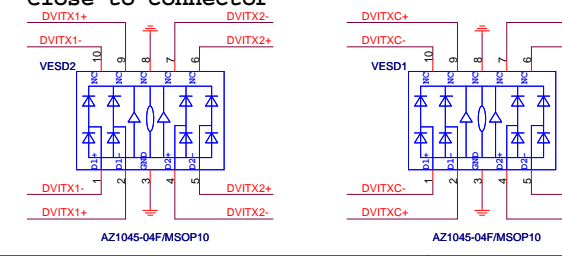
Rev: 0.73

DVI CONN

DVI: 20/4/6/4/20  
Impedance=85 +- 17.5%



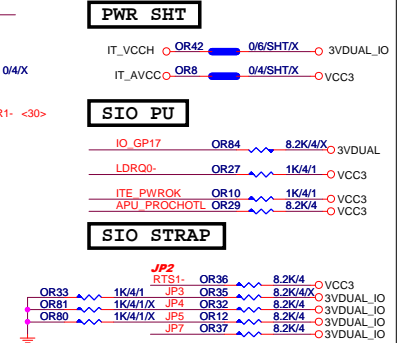
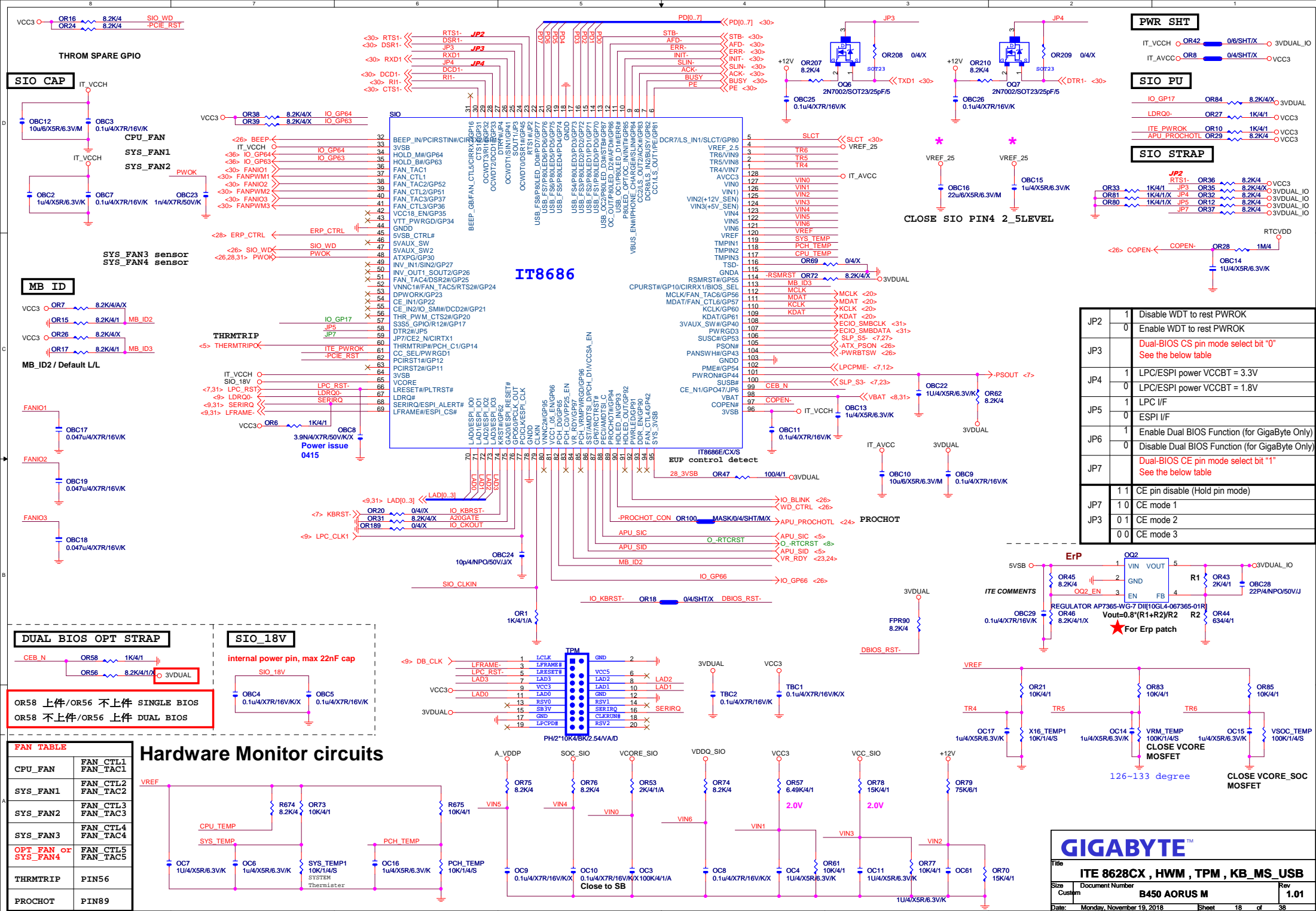
Close to connector



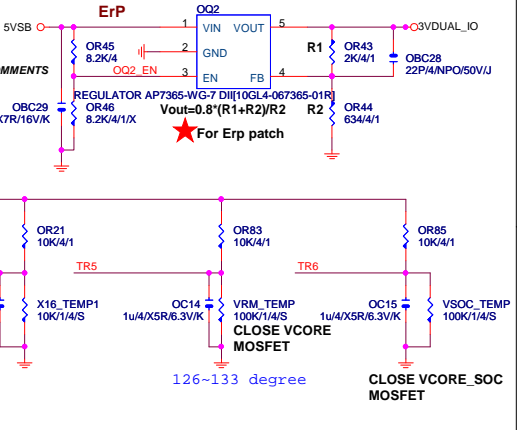
**GIGABYTE**

**HDMI, DVI**

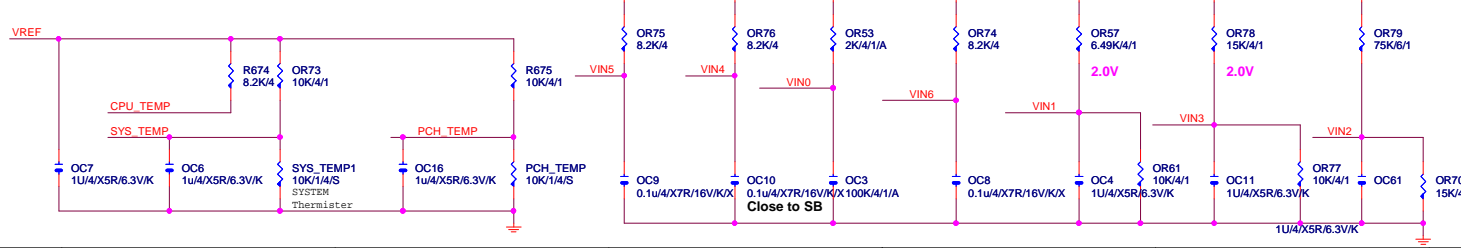
Size: Custom  
Document Number: B450 AORUS M  
Date: Monday, November 19, 2018  
Sheet: 17 of 38  
Rev: 1.01



JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3



### Hardware Monitor circuits

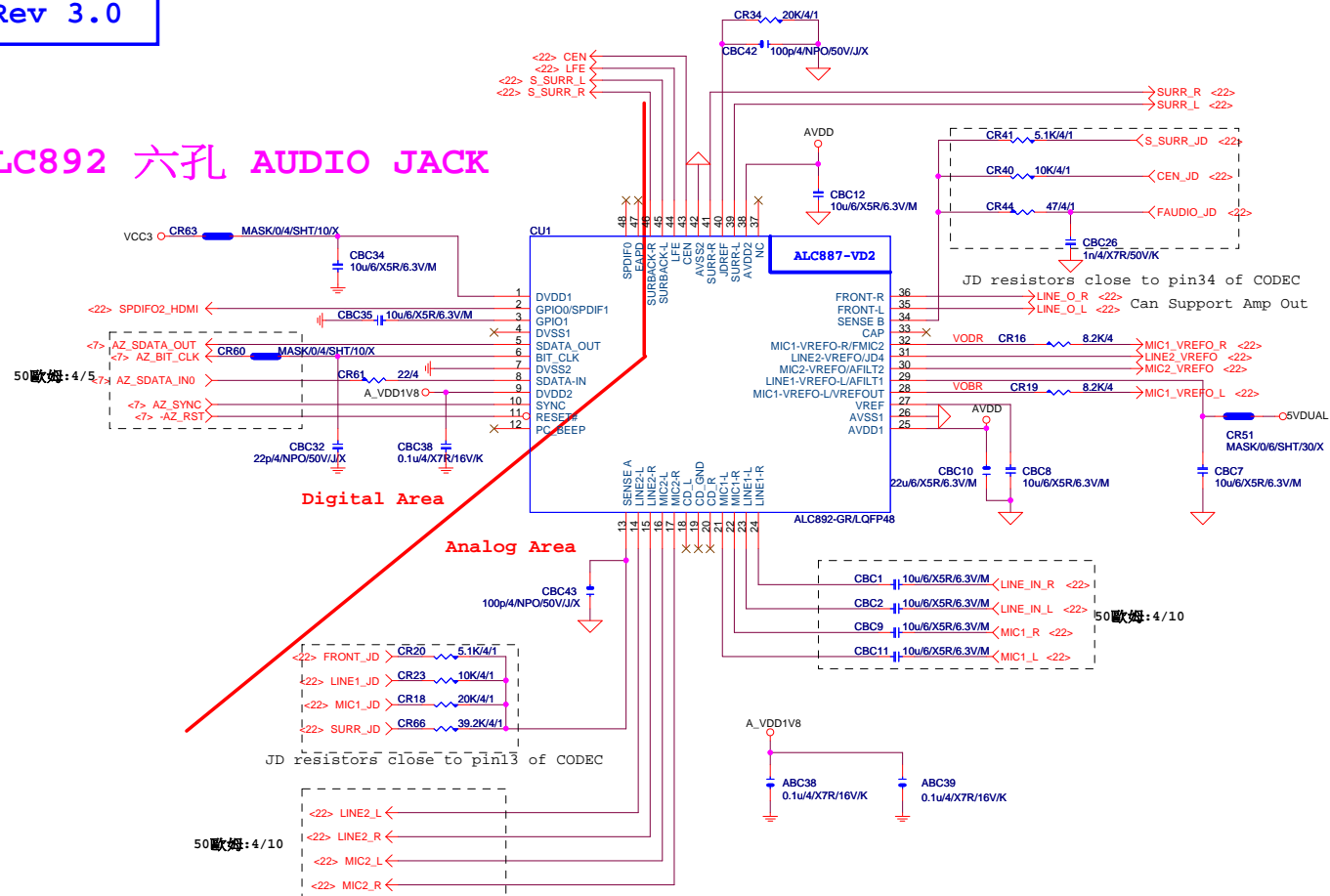






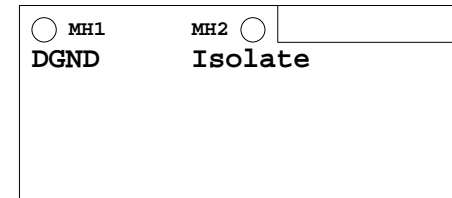
Rev 3.0

# ALC892 六孔 AUDIO JACK



LAYOUT注意: 螺絲孔下GND方式

1. MH1空間夠, 下DGND  
空間不夠, 才改為Isolate
2. MH2一律改為Isolate
3. Codec下方, 第二層必須參考GND



LAYOUT注意: 要加

GND切割線

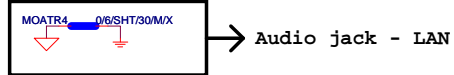
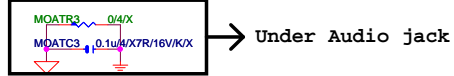
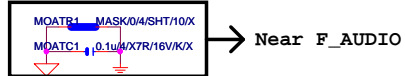
音效區域印刷



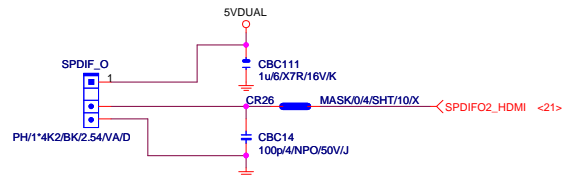
- BOM OPTION :
1. Chemicon音效電容
  2. 金屬外罩 Reserve (LAYOUT上件與否, 依照各Model spec)
  3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

GIGABYTE™			
Title ALC887 CODEC			
Size Custom	Document Number B450 AORUS M		Rev 1.01
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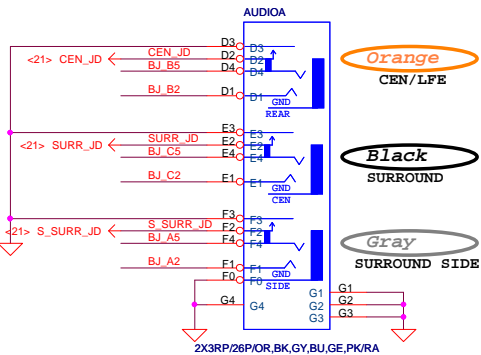
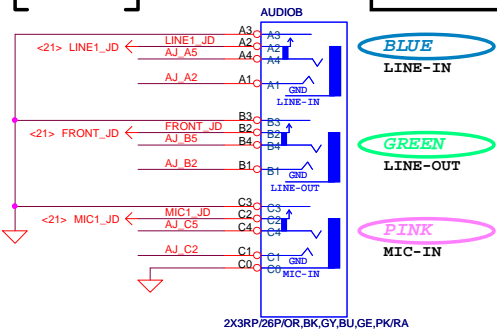
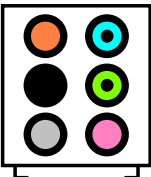
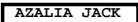
Rev 3.0



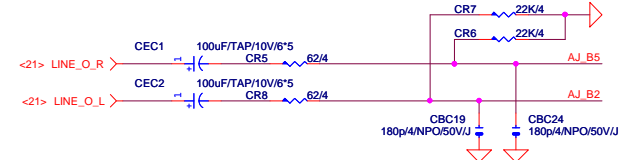
\*量產前, 0ohm改short pad



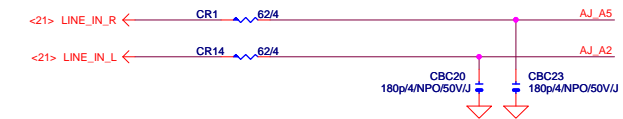
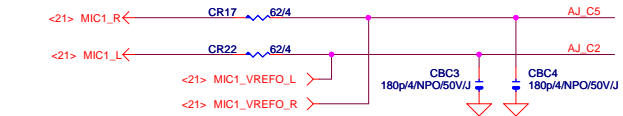
For HDMI SPDIF (依SPEC保留或移除)



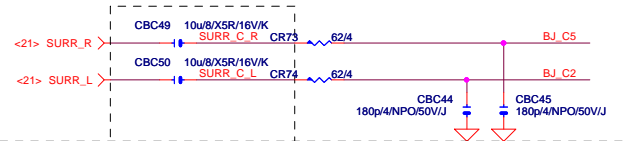
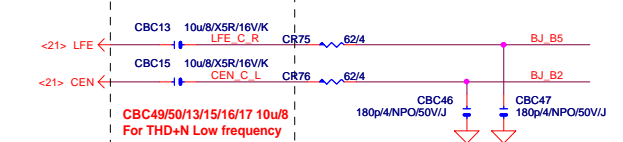
## LINE-OUT



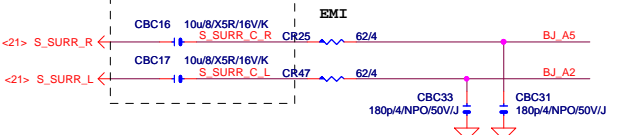
**LINE-IN**

**MIC-IN**

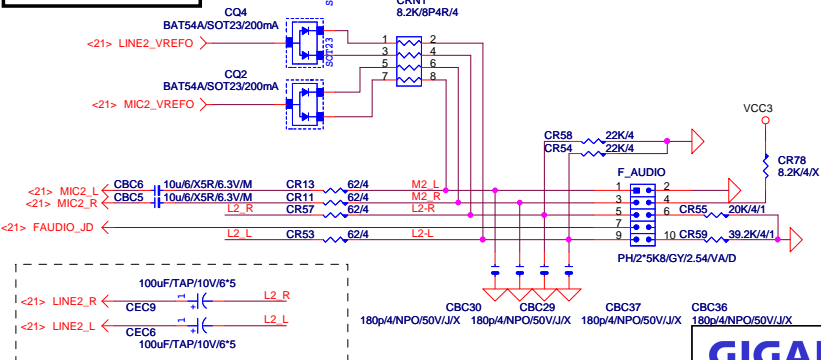
**SURROUND**

**CEN/LFE**

**SURR BACK**



**AZALIA FRONT PANEL**

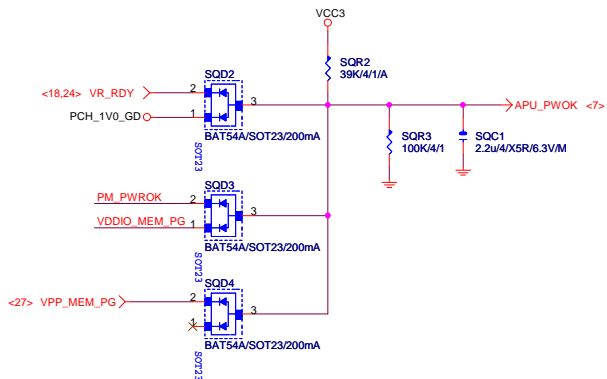


**GIGABYTE™**

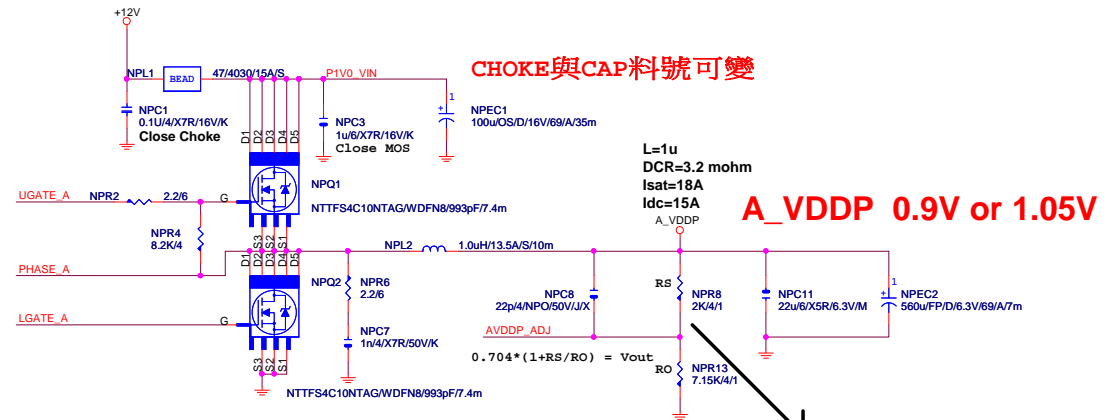
Title	<b>AUDIO JACK</b>
-------	-------------------

Size	Document Number	Rev
Custom	<b>B450 AORUS M</b>	<b>1.01</b>

Date: Monday, November 19, 2018 Sheet 22 of 38



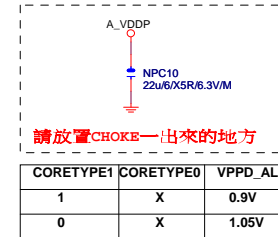
**RF: low=>DEM mode, high=>CCM mode.**



## CHOKES與CAP料號可變

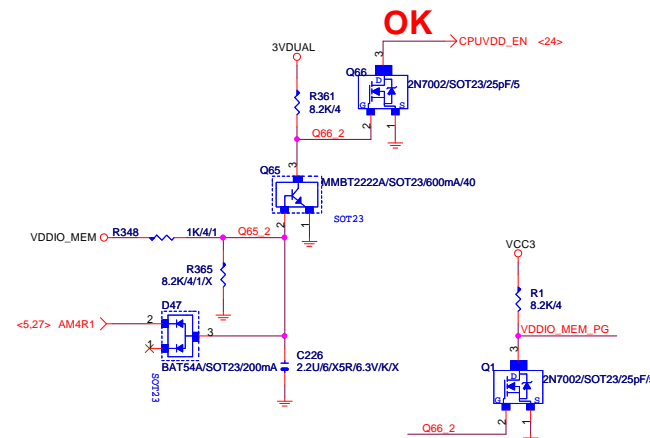
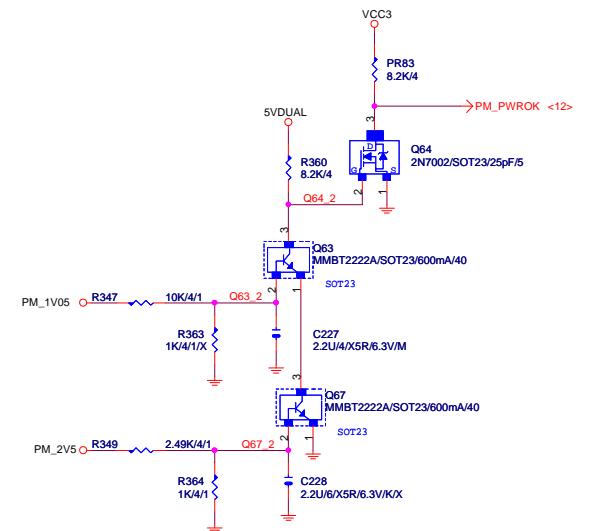
**A\_VDDP 0.9V or 1.05V**

Remote sense請從最重的負載端點拉回



請放置CHOKE一出來的地方

CORETYPE1	CORETYPE0	VPPD_AL
1	X	0.9V
0	X	1.05V



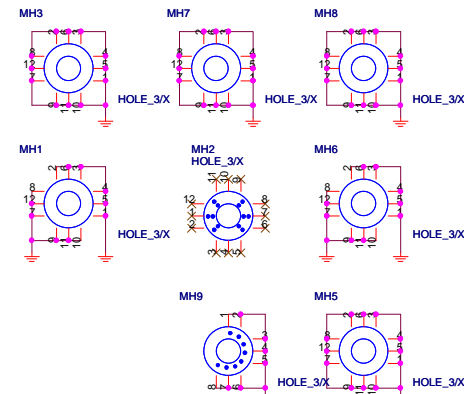
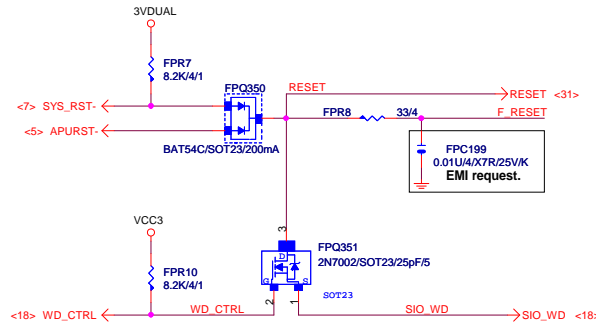
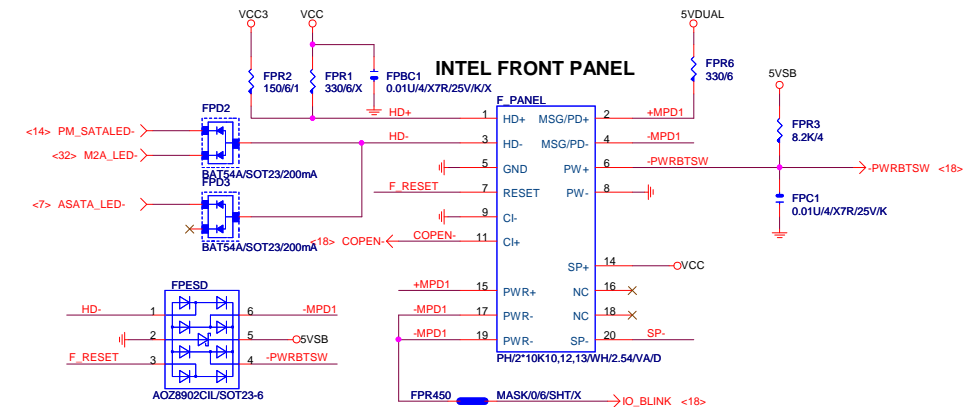




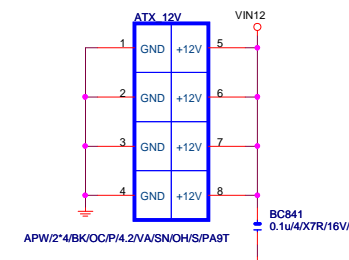
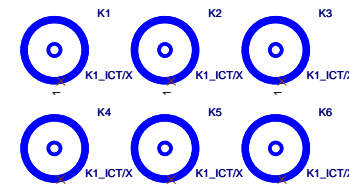




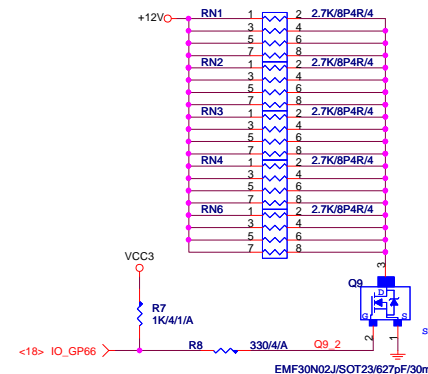
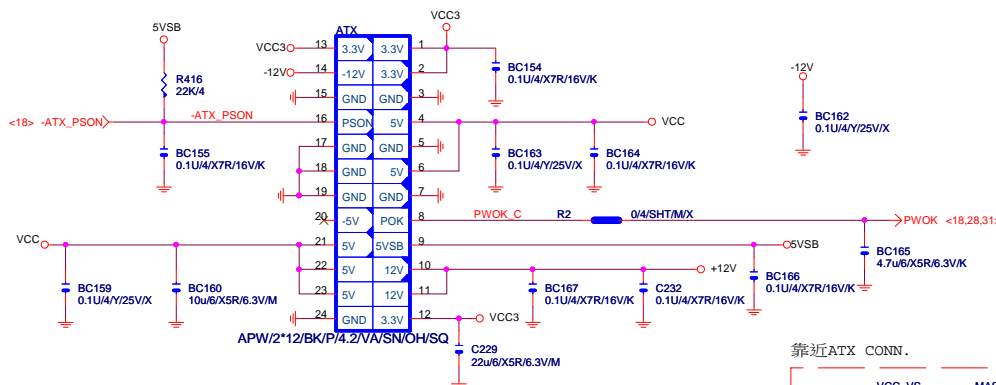
## INTEL FRONT PANEL



1/4 Solder Mask



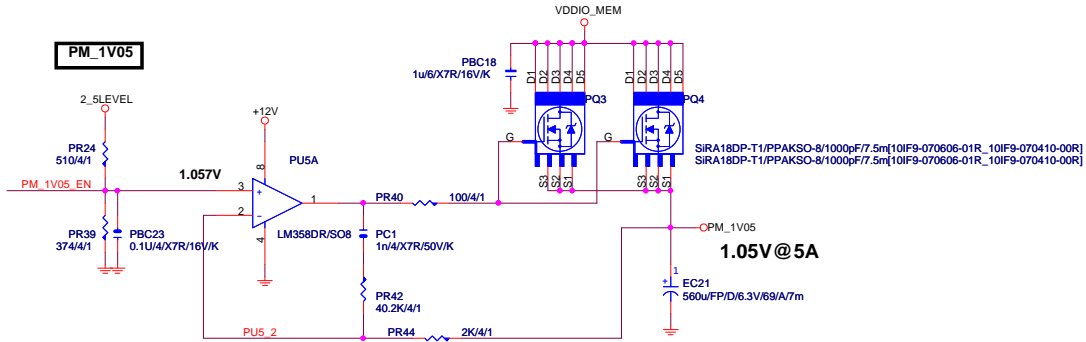
## ATX POWER CONNECTOR



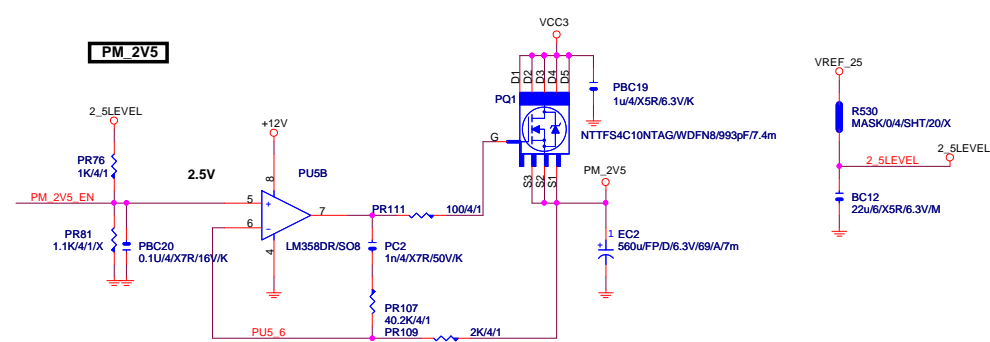
GIGABYTE

Title			
ATX, FRONT PANEL-1			
Size			
Custom	Document Number	B450 AORUS M	Rev 1.01
Date			
Monday, November 19, 2018	Sheet	26	of 38

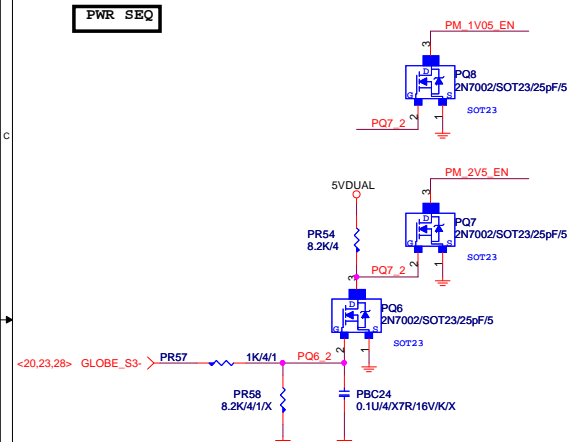
## PM\_1V05



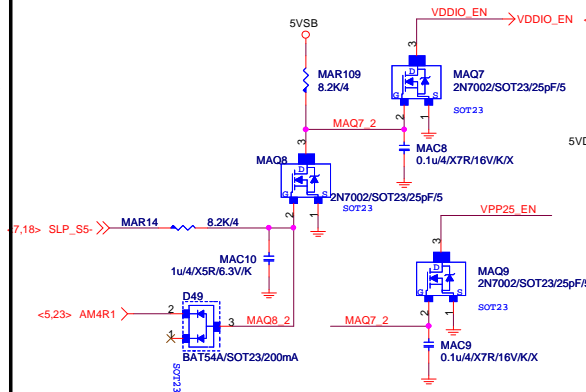
## PM\_2V5



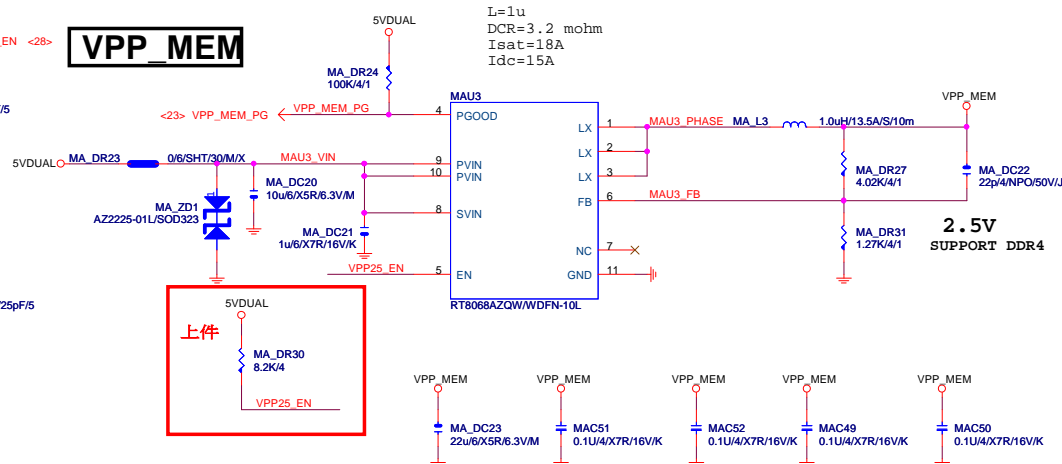
## PWR\_SEQ



## PWR\_SEQ

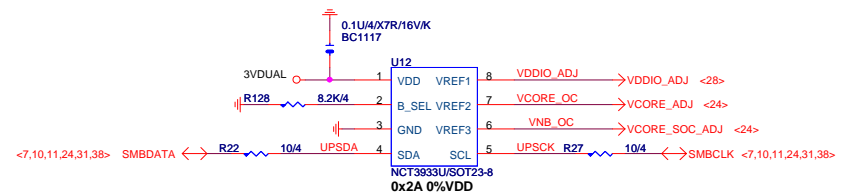
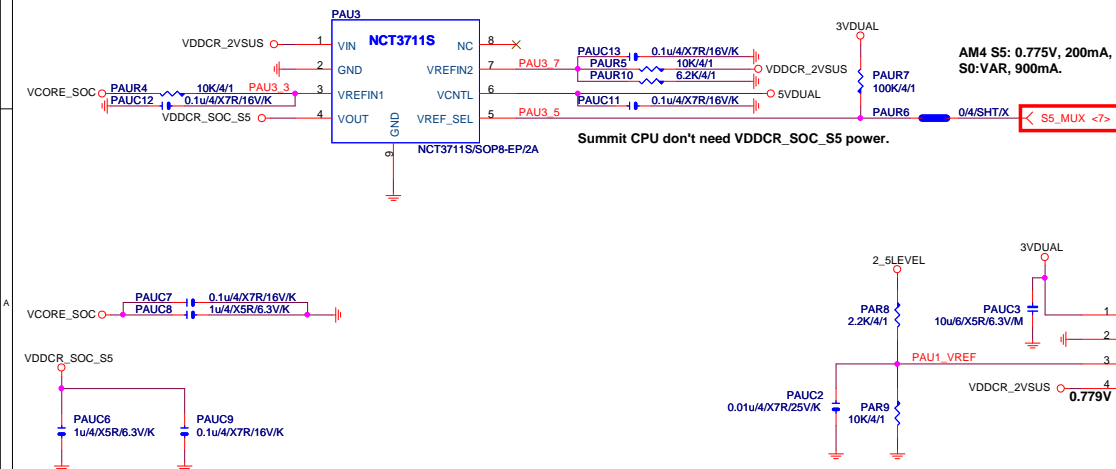


## VPP\_MEM



## VDDCR SOC S5

S5\_MUX: S0-->High, S5-->Low  
H: VDDCR\_SOC\_S5 will track VCORE\_SOC.  
L: If VCORE\_SOC < 0.775V (OR 0.85V), VDDCR\_SOC\_S5=0.775V.  
If VCORE\_SOC>=0.775V (OR 0.85V), VDDCR\_SOC\_S5 will trace VCORE\_SOC.

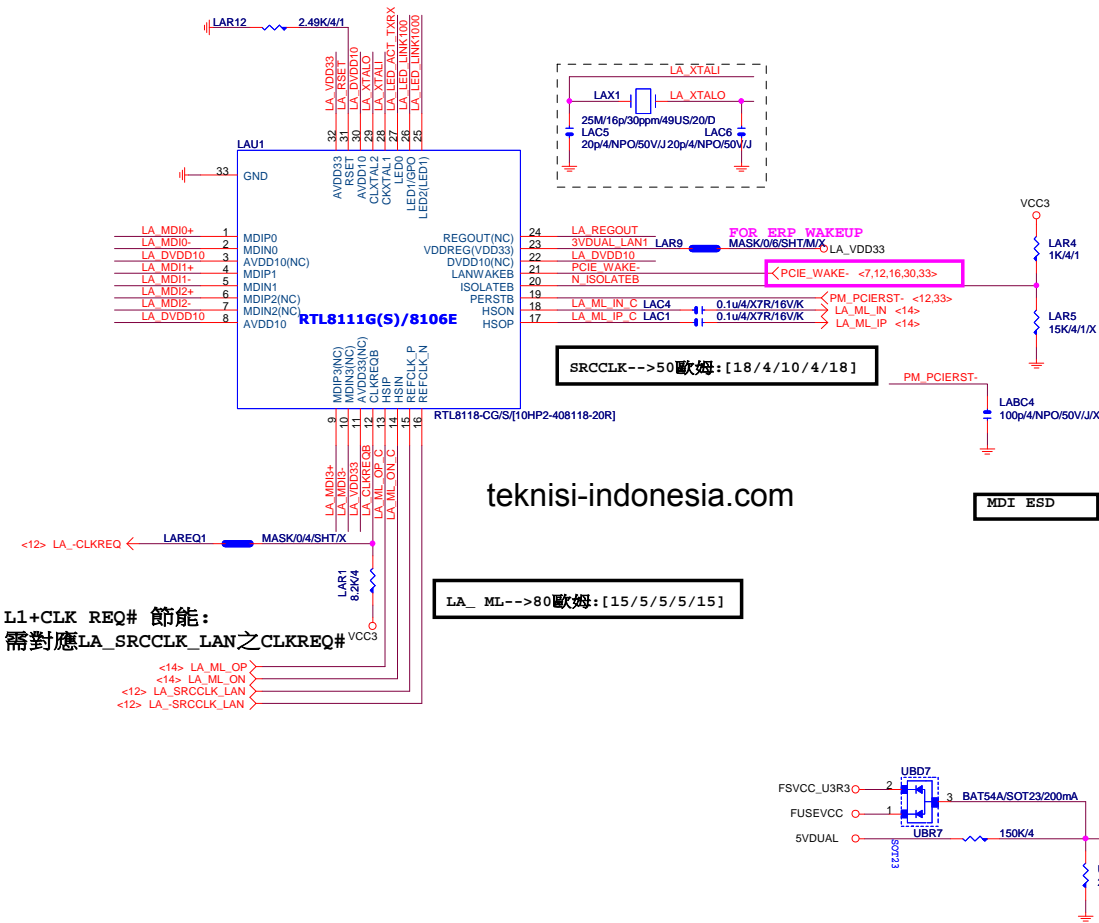


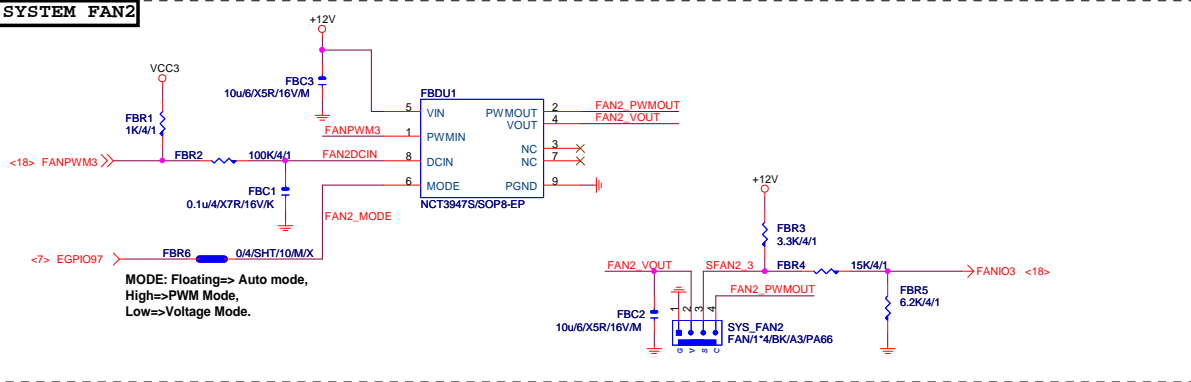
**GIGABYTE**

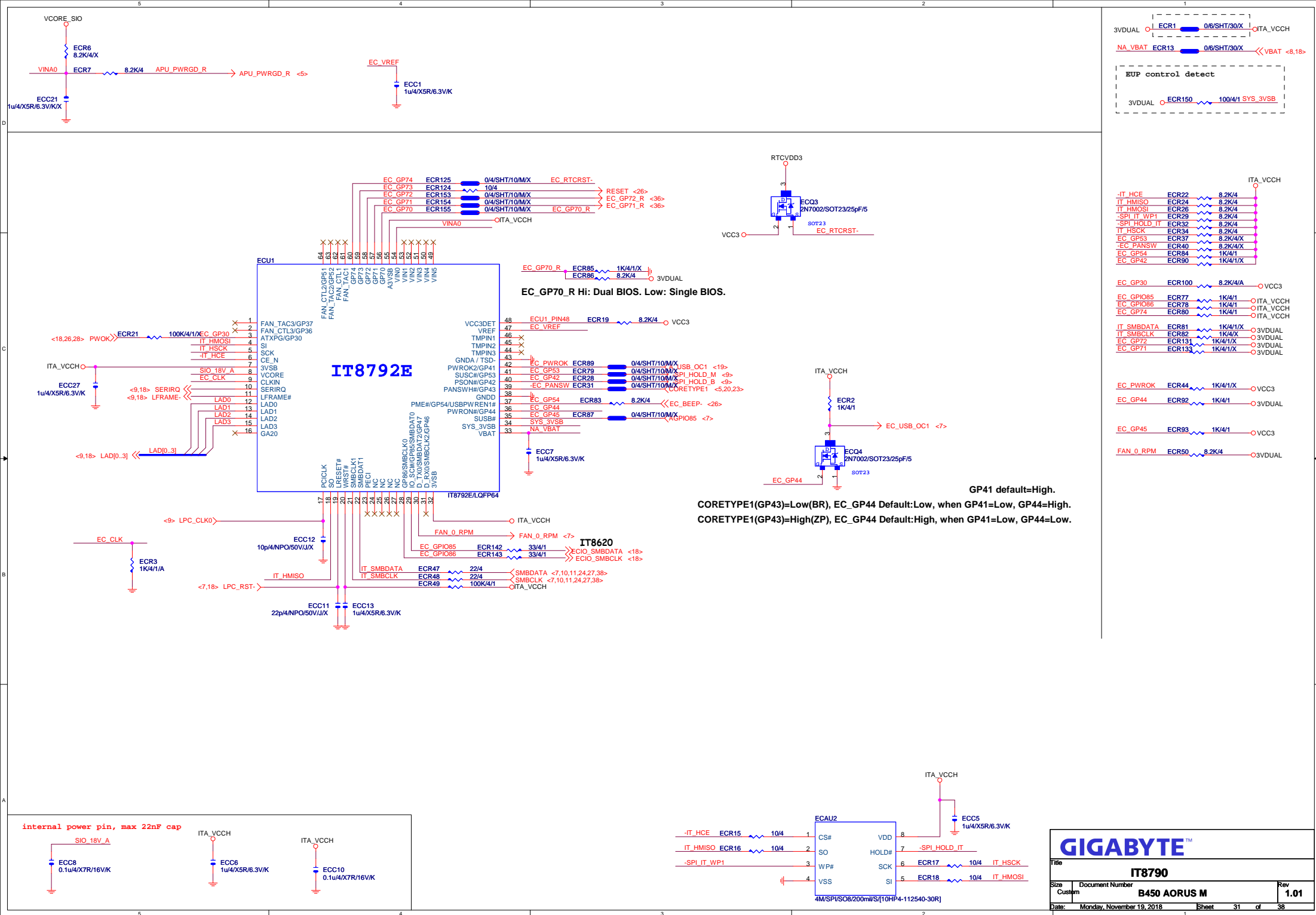
Title			
SB PWR,VDDA25,VCC11DUAL			
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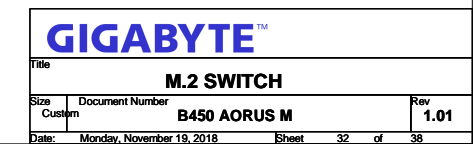
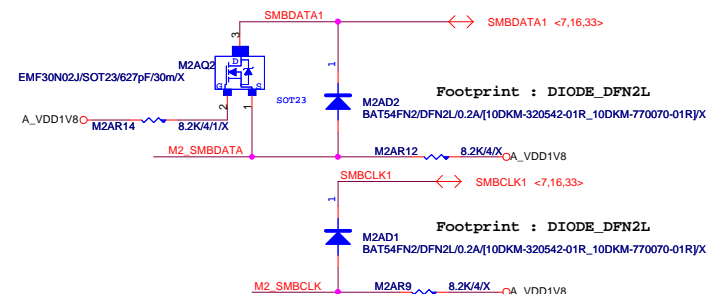
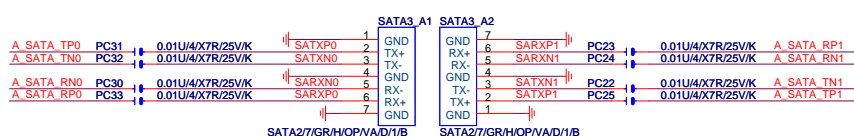
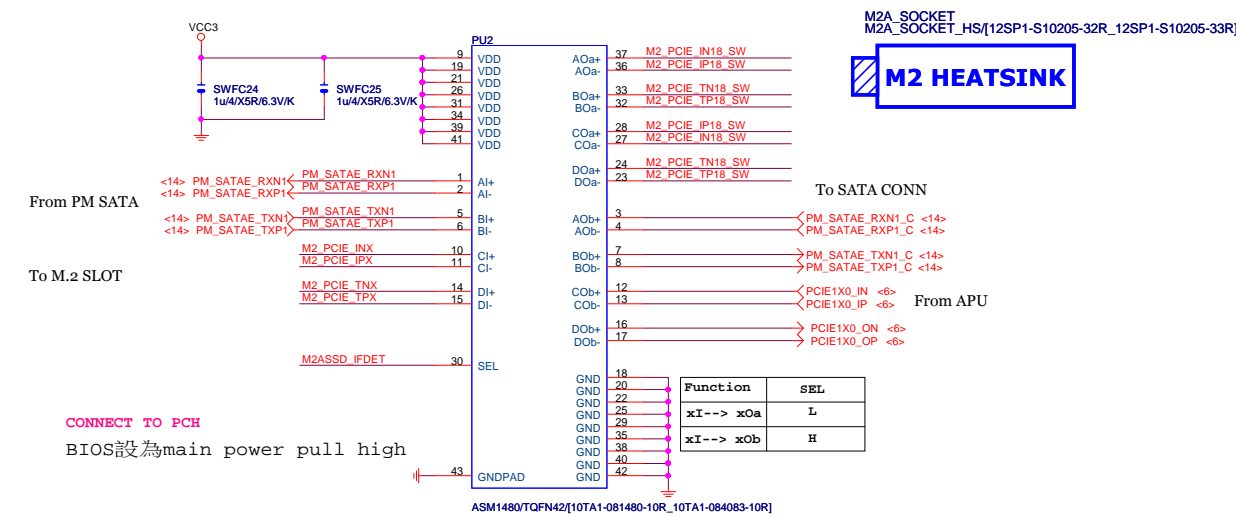
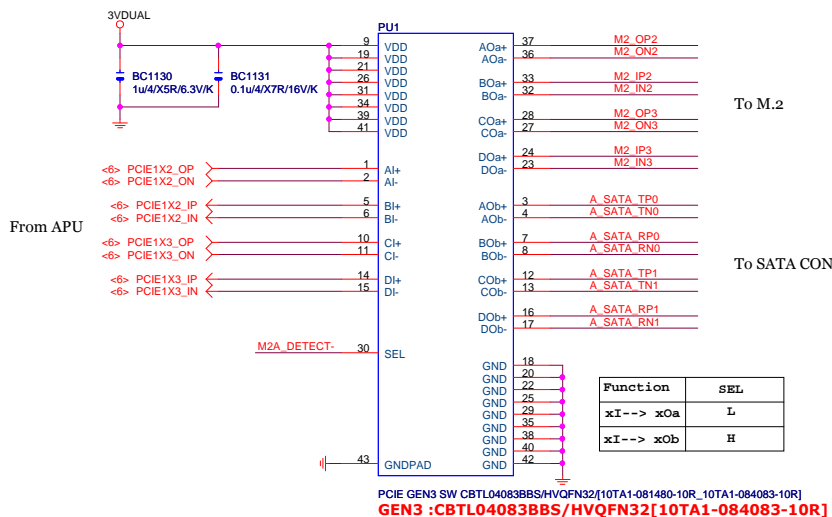
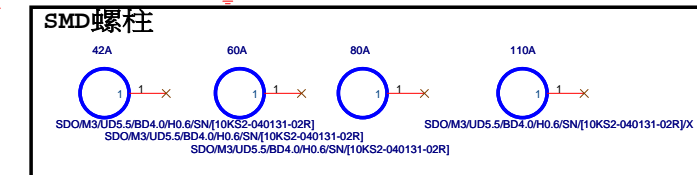
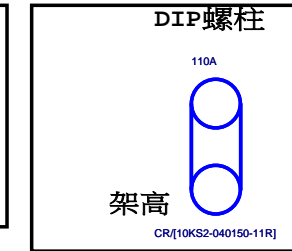
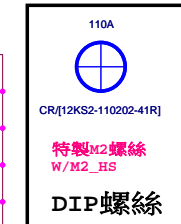
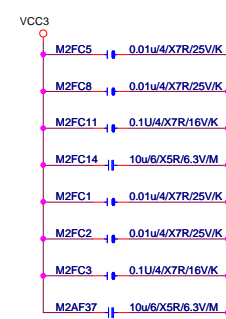
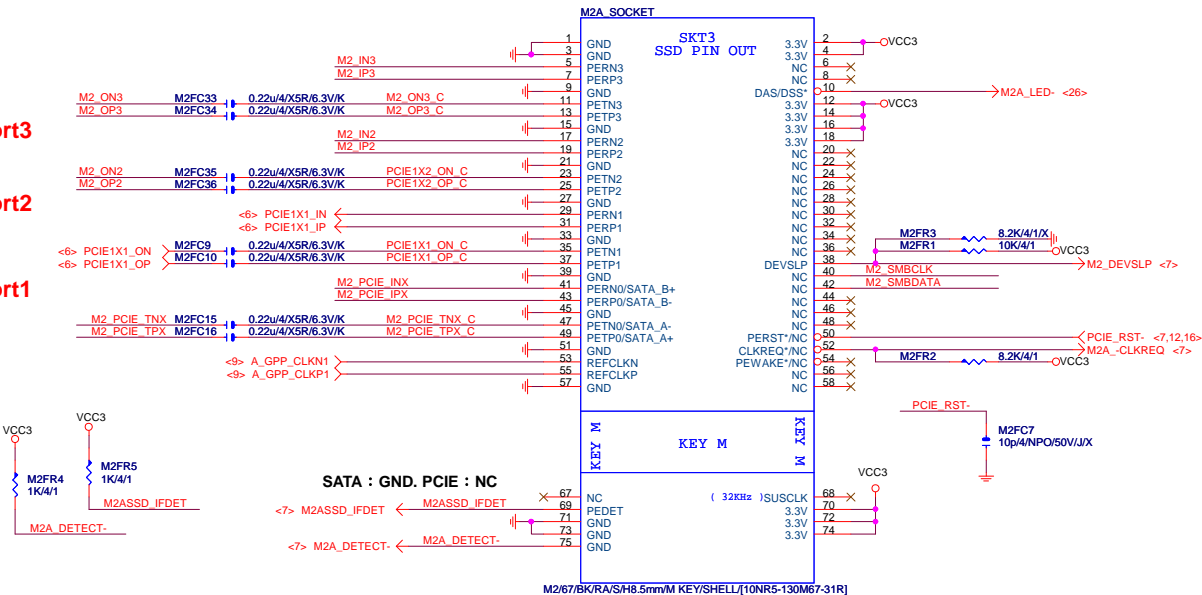
Rev 0.5

### M.2 Lane4 from AM4 port3

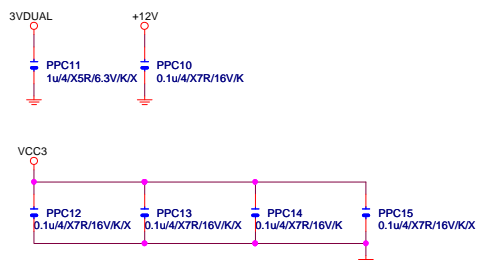
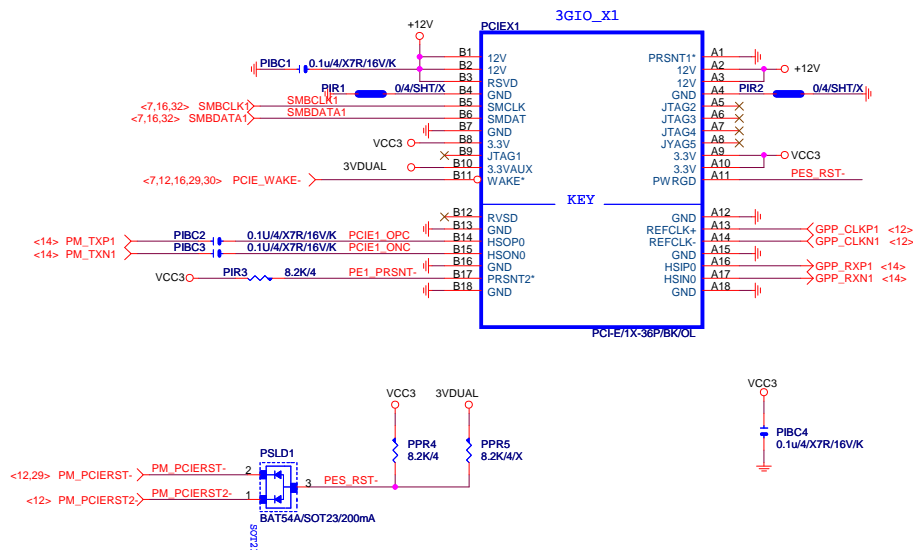
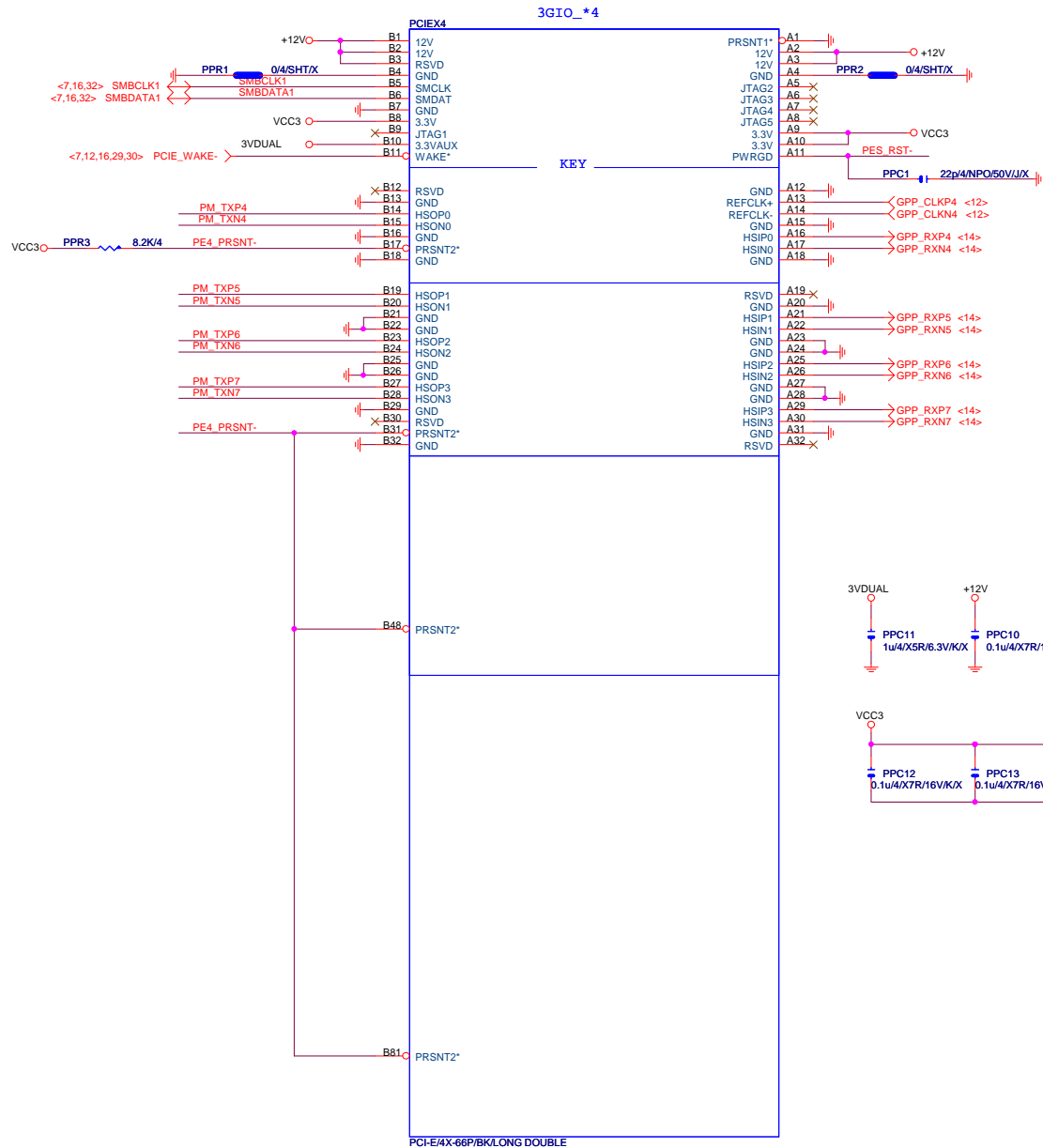
## M.2 Lane4 from AM4 port2

## M.2 Lane4 from AM4 port1

## by SWITCH Select



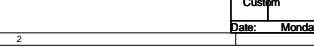
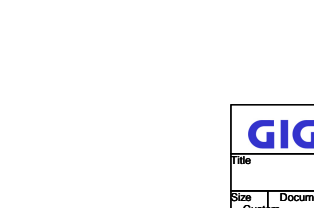
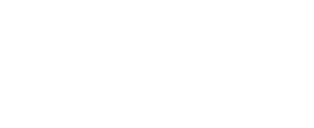
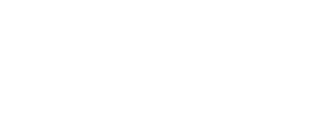
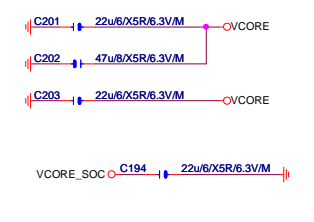
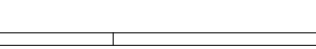
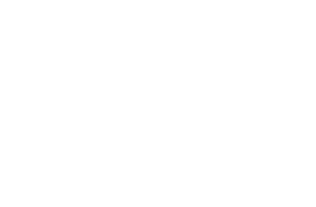
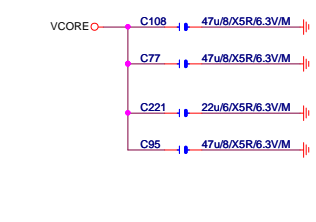
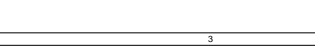
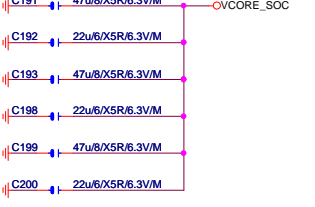
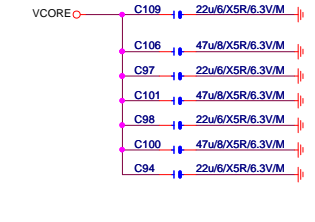
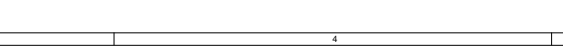
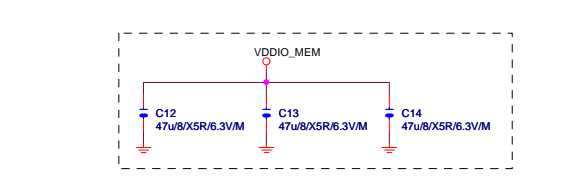
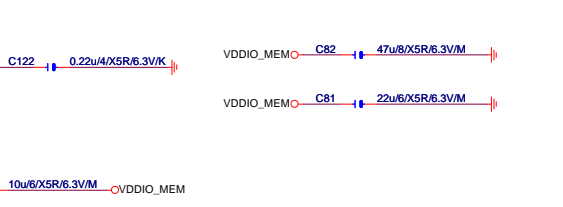
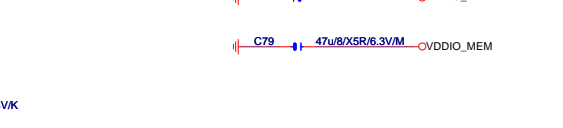
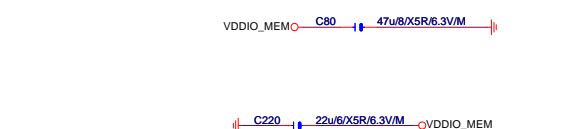
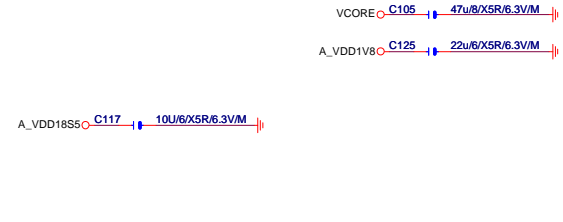
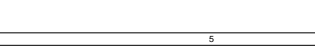
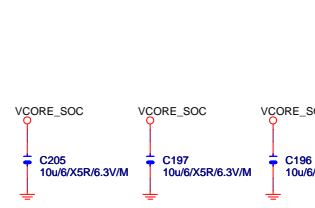
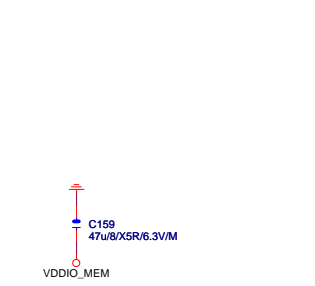
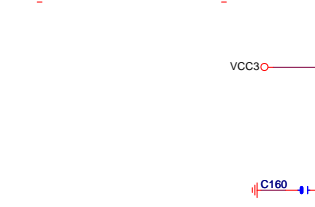
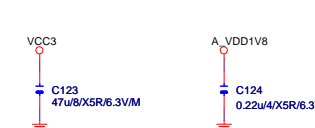
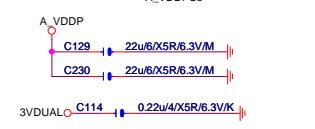
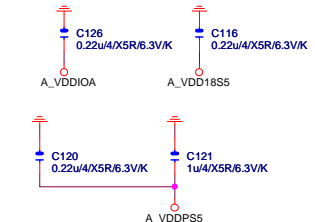
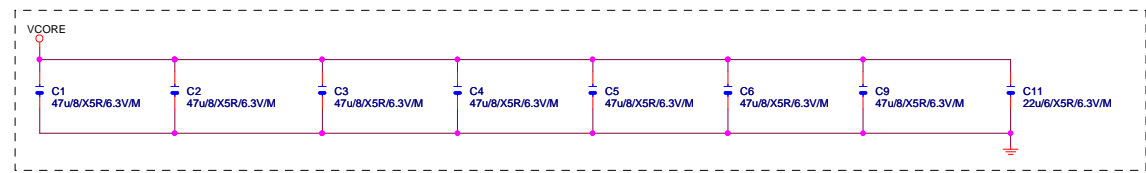




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<14> GPP_TXP4	GPP_TXP4	PPC2	0.1U/4/X7R/16V/K	PM_TXP4
<14> GPP_TXN4	GPP_TXN4	PPC3	0.1U/4/X7R/16V/K	PM_TXN4
<14> GPP_TXP5	GPP_TXP5	PPC4	0.1U/4/X7R/16V/K	PM_TXP5
<14> GPP_TXN5	GPP_TXN5	PPC5	0.1U/4/X7R/16V/K	PM_TXN5
<14> GPP_TXP6	GPP_TXP6	PPC6	0.1U/4/X7R/16V/K	PM_TXP6
<14> GPP_TXN6	GPP_TXN6	PPC7	0.1U/4/X7R/16V/K	PM_TXN6
<14> GPP_TXP7	GPP_TXP7	PPC8	0.1U/4/X7R/16V/K	PM_TXP7
<14> GPP_TXN7	GPP_TXN7	PPC9	0.1U/4/X7R/16V/K	PM_TXN7

<b>GIGABYTE™</b>			
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CPU BOTTOM

Size

Custom

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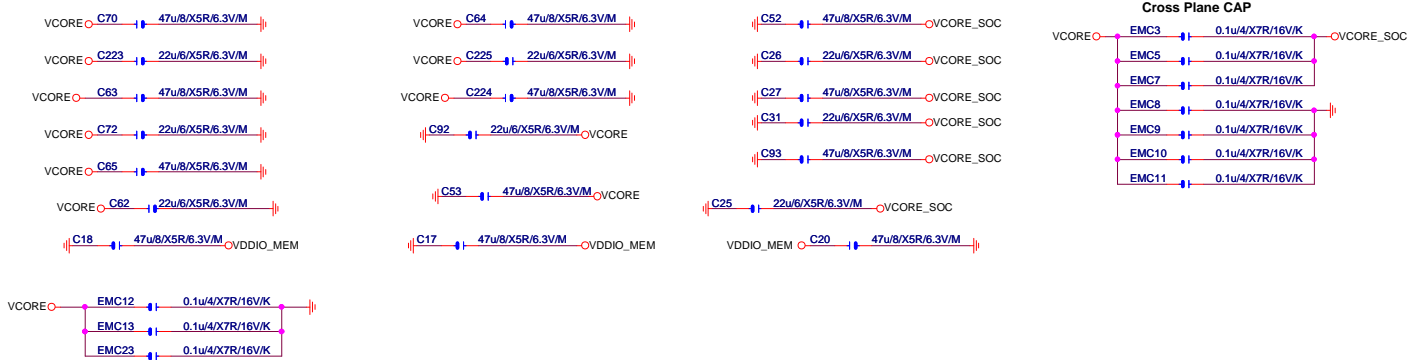
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CPU TOP CAVITY



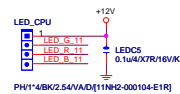
**GIGABYTE™**

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## 第一區 LED

FOR CPU 正發光 LED\*4  
(在CPU CHOKE之間,MOS\_HS下方,不外露)

AMD CPU\_FAN LED connector



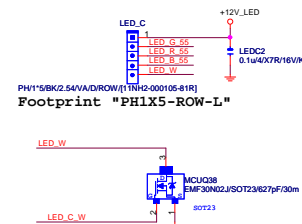
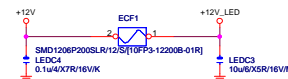
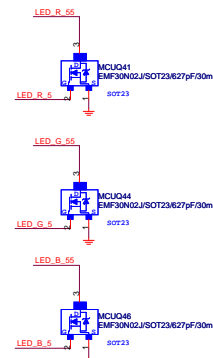
## 第二區 LED

FOR DIMM 側發光 LED\*12  
(位置在DIMM兩側)

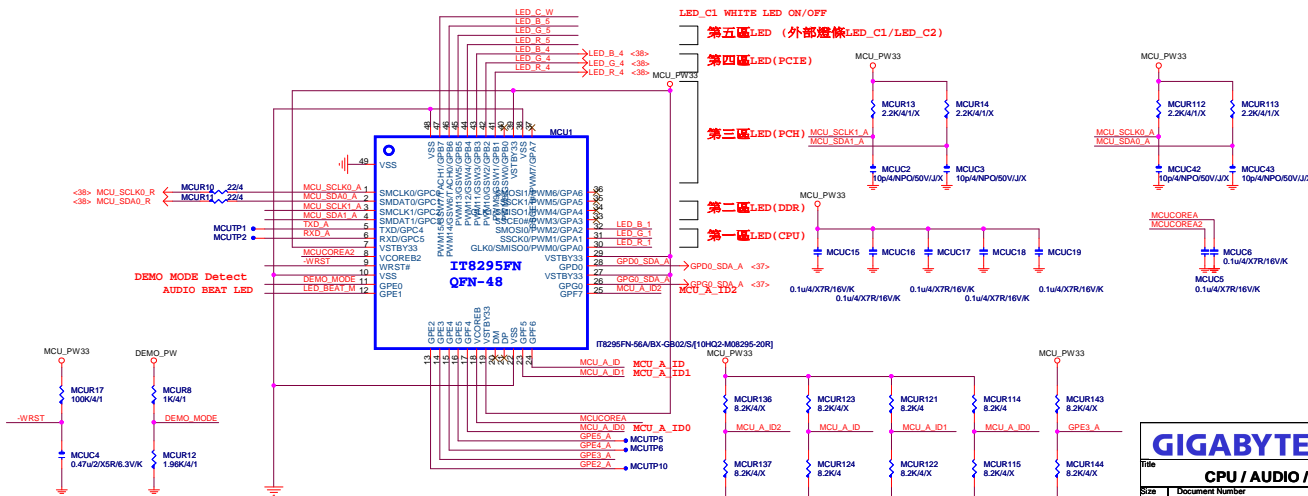
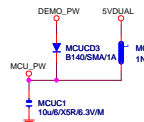
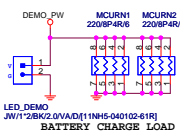
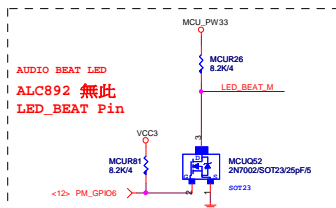
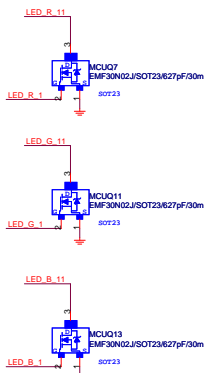
## 第五區 LED

燈條 LED (LED\_C1放在PCB左邊板邊位置)

## 第五區 LED CONTROL



## 第一區 LED CONTROL

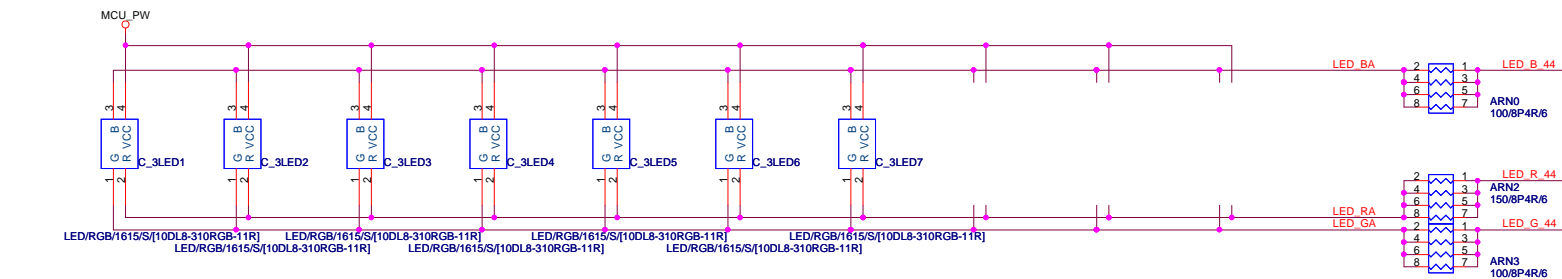




第三區 LED

第四區 LED

FOR AUDIO 正發光 LED\*8 C\_3LED1~8)



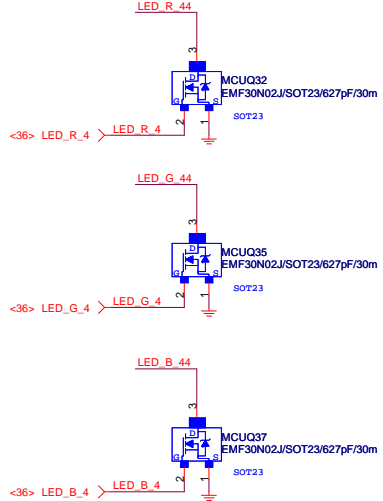
FOOTPRINT:LED-4P-RGB

FOR PCIE16\_1 側發光 LED\*4  
(位置在PCIE16\_1 SLOT兩側各4顆)

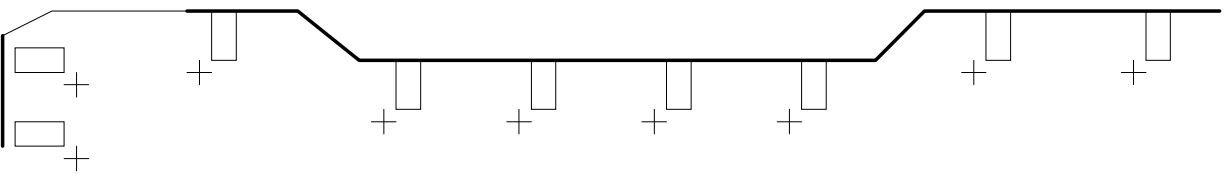
FOR PCIE8 側發光 LED\*4  
(位置在PCIE8 SLOT兩側各4顆)

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第四區 LED CONTROL



Audio Ground切割線+背面 RGB LED



RGB LED LAYOUT 注意事項 :

- 1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
- 2. 背板 RGB LED 方向整板請統一如下  
(整板正極可統一朝下或朝上)
- 3. 正板 RGB LED 統一方向即可
- 4. MCU\_PW & MCU\_PW33電源一律走20mils
- 5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
- 6. MCU LED 出pin的走線4mils,如:LED\_R\_1,LED\_G\_1,LED\_B\_1 .....
- 7. LED RGBW rule :W/S=10/5 mils 如:LED\_R\_11,LED\_G\_11,LED\_B\_11,LED\_W.....  
(包含從晶體到排阻到LED的net)
- 8. Digital LED NET rule W/S=4/8 mils  
GPD0\_SDA\_B,GPD0\_SDA\_BB,GPD0\_SDA\_C,GPD0\_SDA\_CC

For AMD MCU update

